What is claimed is:

Sub B7

1. A memory device comprising:

an array of memory cells arranged in rows and columns, a portion of said memory cells being divided into segments;

a global bias circuit generating a plurality of first bias currents; and

a plurality of local bias networks, each local bias network comprising:

a local bias circuit generating a plurality of second bias currents in response to a corresponding one of the plurality of first bias currents, and

a plurality of segment bias circuits generating a third bias current, each segment bias circuit being adjacent to a corresponding segment of said memory cells.

2. The memory device of claim 1 wherein each segment bias circuit provides a ground feedback signal to said local bias circuit, and said local bias circuit adjusts said second bias current in response to said ground feedback signal.

3. The memory device of claim 2 wherein the local bias circuit and the segment bias circuits each comprises transistors and the ground feedback signal provides a relative bias voltage between said transistors.

4. The memory device of claim 3 wherein said relative bias voltage is a voltage across a gate and a source of said transistors.

5. The memory device of claim 1 wherein each segment bias circuit includes a feedback ground line coupled to the local bias circuit to provides a ground feedback signal, and said local bias circuit adjusts said second bias current in response to said ground feedback signal.

6. The memory device of claim 5 wherein the feedback ground lines of the segment bias circuits are coupled to each other.

7. The memory device of claim 5 wherein the feedback ground lines of the segment bias circuits are coupled to a main ground line.

8. The memory device of claim 1, wherein the segment bias circuits are disposed in geometric positions in the segments.

9. The memory device of claim 8 wherein the geometric position is approximately one-fourth of the distance of the segments and relative to an end of the segment having the highest voltage drop.

10. The memory device of claim 8 wherein the geometric position divides the bias voltage difference in the segment approximately equally.

11. The memory device of claim 1, wherein each of the segment bias circuits are disposed adjacent one of said memory cells in a segment to divide said segment into two portions having an equal voltage drop from said segment bias current to a corresponding end of said segment.

12. The memory device of claim 1 wherein the global bias circuit includes a global trim circuit to adjust the plurality of first bias currents in response to a global trim signal.

13. The memory device of claim 12 wherein each local bias network comprises a local trim circuit to adjust the plurality of second bias currents in response to a local trim signal.

14. The memory device of claim 1 wherein each local bias network comprises a local trim circuit to adjust the plurality of second bias currents in response to a local trim signal.

15. The memory device of claim 1 wherein the local bias circuit comprises an output circuit to switch on and off the second bias current and a clock circuit to provide an overlapping clocks to the output circuit to form a break before make connection to the plurality of segment bias circuits.

16. The memory device of claim 1 wherein the local bias circuit comprises a bias generator comprising an n-type channel bias structure for providing said second bias current.

17. The memory device of claim 16 wherein the n-type channel bias structure comprises a native type transistor and an enhancement type transistor coupled in a self cascoding arrangement.

18. The memory device of claim 17 wherein a drain of the native type transistor is arranged a terminal that provides the second bias current.

19. The memory device of claim 17 wherein a bulk of the native type transistor and the enhancement type transistor is coupled to ground, and the drain of the enhancement type transistor is coupled to a ground feedback line.

20. The memory device of claim 17 wherein a bulk of the native type transistor and the enhancement type transistor is coupled to a ground feedback line, and the drain of the enhancement type transistor is coupled to the ground feedback line.

21. The memory device of claim 1 wherein the local bias circuit comprises an interface coupled to a test point for providing a read current or receiving a write current.

22. A method for biasing an array of memory cells arranged in rows and columns, the method comprising:

dividing a portion of the rows of memory cells into segments;

generating a plurality of global bias currents;

generating a plurality of local bias currents in response to a corresponding one of the plurality of global bias currents; and

generating a plurality of segment bias currents for application to a corresponding one of the segments in response to a corresponding one of the plurality of local bias currents, each segment bias current being generated adjacent to a corresponding segment of said memory cells.

23. The method of claim 22 further comprising:

adjusting ones of said plurality of local bias currents in response to a ground feedback signal from corresponding ones of the segments of memory cells.

24. The method of claim 23 further comprising coupling the feedback ground signal from each segment to each other.

25. The method of claim 23 further comprising coupling the feedback ground signal of the segments to a main ground line.

26. The method of claim 22, further comprising applying the segment bias currents to segments in geometric positions in the segments.

27. The method of claim 26 wherein the geometric position is approximately one-fourth of the distance of the segments and relative to an end of the segment having the highest voltage drop.

28. The method of claim 26 wherein the geometric position divides the bias voltage difference in the segment approximately equally.

29. The method of claim 22, wherein applying each of the segment bias currents to a corresponding segment of said memory cells to divide said segment into two portions having an equal voltage drop from a location of said application of said segment bias current to a corresponding end of said segment.

30. The method of claim 22 further comprising applying a read current to or receiving a write current from a test point to test the plurality of local bias currents.

31. A distributed current network comprising:

a global bias network generating a plurality of local bias drive currents; and

a plurality of local bias networks coupled to the global bias network, each local bias network generating a segment bias current in response to a corresponding one of the plurality of local bias drive currents.

32. The distributed current network of claim 31 wherein the local bias network comprises:

a local bias current generating a segment bias voltage in response to said corresponding one of the plurality of local bias drive currents; and

a plurality of segment biasing currents, each segment biasing current generating a segment bias current in response to said local bias drive current.

33. The distributed current network of claim 32 wherein the plurality of segment biasing circuits includes a ground feedback line coupled to the local bias current circuit and the local bias current circuit further adjusts the local bias drive current based on feedback currents on the ground feedback line.

34. A testing device comprising:

a test pad;

a resistive element having a first terminal coupled to the test pad and having a second terminal;

a first transistor of a first type including a first terminal coupled to the second terminal of the resistive element, including a second terminal spaced apart from said first terminal with a channel therebetween, and including a gate for controlling current in said channel; and

a transfer gate including a first terminal coupled to the second terminal of the first transistor of the first type and including a second terminal coupled to a circuit current terminal.

35. The testing device of claim 34 further comprising:

a second transistor of the first type including a first terminal coupled to the first terminal of the first transistor of the first type, including a second terminal spaced apart from said first terminal with a channel therebetween, and including a gate coupled to the gate of the first transistor of the first type for controlling current in said channel; and

a third transistor of the first type including a first terminal coupled to the second terminal of the second transistor of the first type, including a second terminal coupled to a ground terminal and spaced apart from said first terminal with a channel therebetween, and including a gate coupled to the ground terminal for controlling current in said channel.

36. The testing device of claim 35, wherein the transfer gate comprises:

a plurality of third transistors of the first type, each third transistor of the first type including a first terminal, including a second terminal spaced apart from said first terminal with a channel therebetween, and including a gate for controlling current in said channel, the first and second terminals of the third transistors of the first type being coupled in series between the first terminal of the transfer gate and the second terminal of the transfer gate, the gates of the third transistors of the first type being coupled together and to an enable signal; and

a plurality of first transistors of a second type, each first transistor of the second type including a first terminal, including a second terminal spaced apart from said first terminal with a channel therebetween, and including a gate for controlling current in said channel, the first and second terminals of the first transistors of the second type being coupled in series between the first and second terminals of the transfer gate, the gates of the first transistors of the second type being coupled together and to an inverted enable signal.

37. A memory device comprising:

an array of memory cells arranged in rows and columns;

a first bias circuit generating a bias current; and

a second bias circuit comprising a plurality of bias current sources, each bias current source coupled to a corresponding memory cell and mirroring said bias current.

38. The memory device of claim 37 wherein the first bias circuit includes a current source and a first bias transistor and each bias current source includes a second bias transistor coupled to a corresponding memory cell and is coupled to the first bias transistor to mirror said bias current.

39. The memory device of claim 37 wherein the memory cells are hot electron injection memory cells.

40. The memory device of claim 37 wherein the memory cells are split gate memory cells.